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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,789	01/30/2002	Masatoshi Kokubun	100353-00095	4716

7590 11/02/2005

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EXAMINER	
JELINEK, BRIAN J	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,789	KOKUBUN ET AL.	
	Examiner	Art Unit	
	Brian Jelinek	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,10-14,29 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10-14,29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

The Examiner respectfully submits a response to the amendment received on 8/9/2005 of application no. 10/058,789 filed on 1/30/2002 in which claims 1-4, 11-14, and 29-30 are currently pending.

Remarks

The Examiner appreciates the Applicant's incorporation into the independent claims of limitations objected to in the previous office action. However, upon further search and consideration, a new ground of rejection is made. The Examiner apologizes for any inconvenience to the Applicant.

Claim Objections

Claims 1, 4, and 20 are objected to because of the following informalities.

Claim 1 lacks antecedent basis for the limitation in the claim. The claim recites the limitation "N-channel MQS transistor"; the Examiner suggests "N-channel [[MQS]] MOS transistor".

The claim status of claim 4 is "original".

The claim status of claim 20 is "withdrawn".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maki (U.S. Pat. No. 5,907,357), in view of Erstad (U.S. Pat. No. 6,356,101).

Regarding claim 1, Maki discloses a CMOS sensor circuit (Fig. 10, PMOS transistor Q13 and NMOS transistor Q14) comprising: a photodiode (Fig. 10, diode sensor 40); a reset transistor resetting said photodiode to an initial voltage (Fig. 10, reset transistor 45); and a voltage control circuit controlling a gate potential of said reset transistor to a potential other than power source potentials (Fig. 3A, voltage rs controls the gate potential of the reset transistor to all potentials between a base voltage and Vdd), wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor (Fig. 15, inverter 12), the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal (Fig. 15, transistor Q13), an N-channel MOS transistor having a gate supplied with a second signal (Fig. 15, transistor Q14), and a transistor used for controlling a blooming (Fig. 15, transistor Q15). Maki does not disclose a delay circuit producing said first signal by delaying said second signal.

However, Erstad discloses removing glitches from an inverter circuit using a delay line (Figs. 1 and 2). One of ordinary skill in the art would have provided a delay line in order to eliminate crow-bar current (col. 1-2). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided a

delay circuit producing said first signal by delaying said second signal in order to eliminate crow-bar current.

Regarding claim 2, Maki disclose a CMOS sensor circuit (Fig. 10, PMOS transistor Q13 and NMOS transistor Q14) comprising: a photodiode Fig. 10, diode sensor 40); a reset transistor resetting said photodiode to an initial voltage (Fig. 10, reset transistor 45); and a voltage control circuit keeping a gate potential of said reset transistor from completely becoming off (Fig. 4, the gate potential of the reset transistor is above the gate voltage of the read transistor, i.e. the reset transistor is never completely off; Fig. 3A, voltage rs controls the gate potential of the reset transistor to all potentials between a base voltage that is greater than zero and Vdd), wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor (Fig. 15, inverter 12), the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal (Fig. 15, transistor Q13), an N-channel MOS transistor having a gate supplied with a second signal (Fig. 15, transistor Q14), and a transistor used for controlling a blooming (Fig. 15, transistor Q15). Maki does not disclose a delay circuit producing said first signal by delaying said second signal.

However, Erstad discloses removing glitches from an inverter circuit using a delay line (Figs. 1 and 2). One of ordinary skill in the art would have provided a delay line in order to eliminate crow-bar current (col. 1-2). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided a delay circuit producing said first signal by delaying said second signal in order to eliminate crow-bar current.

Regarding claim 29, Erstad discloses the delay circuit is formed by an even number of inverters (col. 4, line 27, the delay line is non-inverting).

Regarding claim 30, please see the rejection of claim 29.

Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maki (U.S. Pat. No. 5,907,357), in view of Erstad (U.S. Pat. No. 6,356,101), and further in view of Fuji (U.S. Pat. No. 5,768,203).

Regarding claim 3, Maki discloses a voltage control circuit (Fig. 5) comprises: an inverter circuit driving a gate of a reset transistor (Fig. 5, inverter 12), the inverter circuit including a first P-channel MOS transistor (Fig. 5, transistor Q13) and an N-channel MOS transistor (Fig. 5, transistor Q14); and a resister inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor (Fig. 5, resister R).

Maki does not disclose the resistor may be configured as a transistor. However, Fuji discloses a P-MOS transistor acts as a resistor when its gate and drain are connected (col. 5, lines 64-66). One of ordinary skill in the art would have configured a resistor as a P-MOS transistor with its gate and drain connected because it is well known in the art that a P-MOS transistor thus connected acts as a resistor (col. 5, lines 64-66). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel a MOS transistor because it is well known in the art that a P-MOS transistor with its gate and drain connected acts as a resistor.

Regarding claim 4, please see the rejection of claim 3.

Regarding claim 11, please see the rejection of claim 3.

Regarding claim 12, please see the 103 rejection of claim 3.

Regarding claim 13, please see the 103 rejection of claim 3.

Regarding claim 14, please see the 103 rejection of claim 3.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Jelinek whose telephone number is (571) 272-7366. The examiner can normally be reached on M-F 9:00 am - 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached at (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Jelinek
10/20/2005

DAVID L. OMETZ
SUPERVISORY PATENT
EXAMINER